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PTO/SB/21 (03-03)

Approved for use through 04/30/2003. OMB 0651-0031

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TRANSMITTAL FORM

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Total Number of Pages in This Submission

Application Number	10/773,900
Filing Date	02/06/2004
First Named Inventor	Samir Chaudhry
Art Unit	2811
Examiner Name	Unassigned
Attorney Docket Number	Chaudhry 28-20-10-14-4/075903-289

ENCLOSURES (Check all that apply)

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| <input type="checkbox"/> Fee Transmittal Form | <input type="checkbox"/> Drawing(s) | <input type="checkbox"/> After Allowance Communication to a Technology Center (TC) |
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| <input type="checkbox"/> Response to Missing Parts/Incomplete Application | Remarks | |
| <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53 | | |

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual	John L. DeAngelis, Jr., Esquire, Reg. No. 30,622
Signature	Beusse Brownlee Wolter Mora & Maire, P.A.
Date	May 18, 2004

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on this date: 05/18/2004

Typed or printed	Pamela A. Pagel	Date	05/18/2004
Signature	Pamela A. Pagel		

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: **Samir Chaudhry, et al**

Group Art Unit: **2811**

Serial No.: **10/773,900**

Examiner: **Unassigned**

Filed: **02/06/2004**

Confirmation No.: **8328**

Atty. Docket No.: **Chaudhry 28-20-10-14-4/075903-289**

For: **Vertical Replacement-Gate Silicon-on-Insulator Transistor**

INFORMATION DISCLOSURE STATEMENT

- ☒ 1. Pursuant to 37 CFR 1.97(b)
(within 3 months of filing or prior to 1st Office Action)
- ☐ 2. Certification Pursuant to 37 CFR 1.97(c)
(before Final Office Action or Allowance)
- ☐ 3. Fee Payment Pursuant to 37 CFR 1.97(c)
(before Final Office Action or Allowance)
- ☐ 4. Petition, Certification & Petition Fee Payment Pursuant to 37 CFR 1.97(d) (before issue fee payment)

May 18, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following are submitted in the above identified application in compliance with 37 CFR 1.97 and 1.98:

- ☒ 5. A list of documents on form PTO-1449 together with copies of each identified document and a translation or a concise explanation of each non-English language document is enclosed herewith.

This paper is submitted in accordance with:

- ☒ 6. 37 CFR 1.97(b): [within 3 months of filing or prior to 1st Office Action];
- ☐ 7. 37 CFR 1.97(c): [before Final Office Action or Allowance, whichever is earlier; and
- ☐ 8. The required certification made in item 11 below; or



☐ 9. The \$240.00 fee specified in 37 CFR §1.17(p) for submission of this Information Disclosure Statement is authorized in item 14 below.

☐ 10. 37 CFR § 1.95(d): [before issue fee payment]; and

a) This is a petition for consideration of the subject Information Disclosure Statement. The petition fee (\$130.00) required by 37 CFR 1.17(i)(1) is enclosed via check. (Direct this letter to: "Attention PETITIONS EXAMINER" and if applicable include batch locator information: e.g. "Allowed Files, Batch _____, Date of Allowance _____"), and

b) The required Certification is stated in item 11 below.

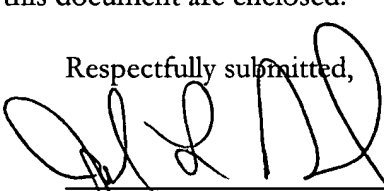
☐ 11. Certification

☐ 12. Each item of information contained in this Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement; or

☐ 13. No item of information contained in this Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing this document after making reasonable inquiry, was known to any individual designated in 37 CFR 1.56(c) more than three (3) months prior to the filing of this Statement.

☐ 14. Please charge all applicable fees associated with the submittal of this Information Disclosure Statement to Deposit Account No. _____.

An original and two (2) copies of this document are enclosed.

Respectfully submitted,


John L. DeAngelis, Jr., Esquire
Reg. No. 30,622
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Orlando, FL 32801
(407) 926-7710

CERTIFICATE OF MAILING

I HEREBY CERTIFY that this Information Disclosure Statement is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 18 day of May, 2004.



Pamela A. Pagel



PTO/SB/08A (08-03)

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Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	10/773,900
Filing Date	02/06/2004
First Named Inventor	Samir Chaudhry
Art Unit	2811
Examiner Name	Unassigned
Attorney Docket Number	Chaudhry 28-20-10-14-4/075903-289

Sheet 1 of 2

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	A	US- 4,366,495	12-28-1982	Goodman, et al	
	B	US- 4,455,565	06-19-1984	Goodman, et al	
	C	US- 4,587,713	05-13-1986	Goodman, et al	
	D	US- 4,683,643	08-04-1987	Nakajima, et al	
	E	US- 4,786,953	11-22-1988	Morie, et al	
	F	US- 4,837,606	06-06-1989	Goodman, et al	
	G	US- 5,342,797	08-30-1994	Sapp, et al	
	H	US- 5,414,289	05-09-1995	Fitch, et al	
	I	US- 5,576,238	11-19-1996	Fu	
	J	US- 5,668,391	09-16-1997	Kim, et al	
	K	US- 5,744,846	04-28-1998	Batra, et al	
	L	US- 6,027,975	02-22-2000	Hergenrother, et al	
	M	US- 6,072,216	06-06-2000	Williams, et al	
	N	US- 6,121,077	09-19-2000	Hu, et al	
	O	US- 6,133,099	10-17-2000	Sawada	
	P	US- 6,197,641	03-06-2001	Hergenrother, et al	
	Q	US- 6,297,531	10-02-2001	Armacost, et al	
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known			
		Application Number	10/773,900		
		Filing Date	02/06/2004		
		First Named Inventor	Samir Chaudhry		
		Art Unit	2811		
		Examiner Name	Unassigned		
Sheet	2	of	2	Attorney Docket Number	Chaudhry 28-20-10-14-4/075903-289

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1	DUDEK, ET AL, "Lithography-Independent Nanometer Silicon MOSFET's on Insulator", IEEE Transactions on Electron Devices, Vol. 43, No. 10, October 1996, pp. 1626-1631.	
	2	RISCH, ET AL, "Vertical MOS Transistors with 70 nm Channel Length", IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1495-1498.	
	3	TAKATO, ET AL, "Impact of Surrounding Gate Transistor (SGT) for Ultra-High-Density LSI's", IEEE Transactions on Electron Devices, Vol. 38, No. 3, March 1991, pp. 573-577.	
	4	TAKATO, ET AL, "High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSIs", IEDM 1988, pp. 222-225.	
	5	HERGENROTHER, ET AL, "The Vertical Replacement-Gate (VRG) MOSFET: A 50-nm Vertical MOSFET with Lithography-Independent Gate Length", Technical Digest of IEDM, 1999, pp. 75-78.	
	6	OH, ET AL, "50 nm Vertical Replacement-Gate (VRG) pMOSFETs", IEEE 2000.	
	7	HERGENROTHER, ET AL, "The Vertical Replacement-Gate (VRG) MOSFET: A High Performance Vertical MOSFET with Lithography-Independent Critical Dimensions", no publication information apparent from document.	
	8	MONROE, ET AL, "The Vertical Replacement-Gate (VRG) Process for Scalable, General-purpose Complementary Logic", Paper 7.5, pp. 1-7, date and publication information unknown.	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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